



IN-LINE WAFER SURFACE MAPPING

FIELD OF THE INVENTION

[0001] The present invention relates, most generally, to semiconductor devices and methods for forming the same. More particularly, the present invention relates to a method and apparatus for mapping raw substrate topography during in-line processing.

BACKGROUND

[0002] Semiconductor devices such as integrated circuits and the like, are formed by performing a series of processing operations upon a substrate to form accurately sized and precisely aligned device features. The device features are formed from various conductive and dielectric films that are formed on the substrate. The processing operations include multiple photolithographic patterning processes used to pattern the various conductive and dielectric films and also to define regions in the films or the substrate into which various impurities will be introduced. It is critical to accurately define the various device features so that they are accurately sized, positioned and aligned to tight tolerances.

[0003] In each of the multiple photolithographic patterning processes, it is critical to project the photolithographic image onto a focal plane that is at a known location such as the substrate surface. If the substrate surface is not at the expected location, pattern distortion and/or misalignment may result. If the substrate surface is not uniformly level, then such pattern distortion and/or misalignment may occur at various locations across the substrate. Many other of the processing operations used to form the various device features are similarly sensitive to the position of the substrate surface. In summary, non-uniformities in the substrate surface can translate to improperly sized, positioned and aligned device features throughout the substrate. This may result in device characteristics that fail and/or vary unacceptably across the substrate.

[0004] It is therefore important for the substrate surface to be uniformly level and likewise important to be able to monitor the topographical uniformity of the substrate

surface. This is especially true as device feature sizes shrink into the nanometer regime while substrate sizes increase to 12 inch diameters or greater, increasing the likelihood that substrate surface non-uniformities will result in device feature defects. It would be especially useful to be able to obtain such topographical data on the raw substrate, during the in-line processing of the substrate and responsive to the detection of unacceptable or non-uniform device parameters or characteristics. Such timely information would be useful in establishing a correlation between these parameters or characteristics, and the substrate topography, or in determining another root cause of the problem. The acquisition of in-line surface topographical data would also be useful in determining the degree of substrate surface non-uniformity that is acceptable for production use. This applies to the various substrates upon which semiconductor devices are formed such as silicon wafers, gallium arsenide wafers, sapphire wafers, and other substrates.

[0005] FIGS. 1A and 1B are exemplary scans of raw substrate surface profiles showing a substrate with an acceptably level profile in FIG. 1A and an unacceptable substrate with extreme undulations shown in FIG. 1B. While "acceptable" versus "unacceptable" is an arbitrary and relative designation, it is apparent that the substrate depicted graphically in FIG. 1A has a relatively uniform surface and also that the substrate depicted graphically in FIG. 1B exhibits relatively poor uniformity. Referring to the substrate depicted graphically in FIG. 1B, it would appear that patterning and other inconsistencies will be produced between devices and features formed in the relatively low areas 101 and those formed in the relatively high areas 103 of such a substrate.

[0006] According to existing technological capabilities, the topography of a substrate is detected and mapped when the substrate is in raw form, *i.e.*, prior to the various manufacturing processing operations carried out upon the substrate. It would therefore be useful to provide a method for mapping the topography of the raw substrate while in-line processing operations are being carried out on the substrate especially since anomalies or non-uniformities are commonly detected during the in-line formation of the devices. The generation of such in-line mapping data can be useful in

determining root cause effects of the various anomalies and in instituting immediate fixes and/or other process controls.

SUMMARY OF THE INVENTION

[0007] To achieve these and other objects, and in view of its purposes, the present invention addresses the shortcomings of conventional technology and provides a method and apparatus for generating topographical data regarding a raw substrate during the in-line processing of the substrate.

[0008] In one exemplary embodiment, the present invention provides a method for mapping surface topography of a substrate. The method comprises forming a non-metallic film over a substrate and a metal film over the non-metallic film. The method further comprises polishing to remove at least a portion of the metal film and distinguishing first regions in which the metal remains from second regions in which the metal has been removed and the non-metallic film exposed. In another exemplary embodiment, the method may be used to distinguish a reflective film from a non-reflective film.

[0009] In another exemplary embodiment, the present invention provides an apparatus for in-line monitoring of surface topography of a substrate. The apparatus includes a body for receiving a substrate thereon, polishing means for polishing a surface of the substrate, and detecting means for detecting the presence or absence of a reflective film, at a plurality of locations on the surface, during the polishing operation.

BRIEF DESCRIPTION OF THE DRAWING

[0010] The present invention is best understood from the following detailed description when read in conjunction with the accompanying drawing. It is emphasized that, according to common practice, the various features of the drawing are not necessarily to scale. On the contrary, the dimensions of the various features are arbitrarily expanded or reduced for clarity. Like numerals denote like features throughout the specification and drawing. Included are the following figures:

[0011] FIGS. 1A and 1B are plots of substrate topography for acceptable and unacceptable substrates respectively;

[0012] FIG. 2 is a plan view of an exemplary substrate with an uneven substrate surface and an accompanying topographical plot that is representative of the uneven surface;

[0013] FIG. 3 is a cross-sectional view of an exemplary substrate with an uneven substrate surface;

[0014] FIG. 4 is a cross-sectional view showing the exemplary substrate in FIG. 3 after a film has been formed over the substrate;

[0015] FIG. 5 is a cross-sectional view showing a non-metallic film formed over the structure shown in FIG. 4;

[0016] FIG. 6 is a cross-sectional view showing a metal film formed over the structure shown in FIG. 5 after ;

[0017] FIG. 7 is a cross-sectional view showing the exemplary substrate shown in FIG. 6 during a subsequent polishing operation according to the present invention;

[0018] FIG. 8 is a partial plan view of a substrate surface containing semiconductor devices and scribe lines; and

[0019] FIG. 9 is a schematic view of an exemplary in-line monitoring apparatus.

DETAILED DESCRIPTION

[0020] FIG. 2 is a plan view that illustrates an uneven substrate surface of an exemplary substrate. Alternatively stated, the substrate surface has a non-uniform topography. The topography of the uneven surface is represented by plot 11 which is taken along arbitrary direction 12 in the exemplary embodiment. The higher and lower sections in plot 11 correspond to raised and depressed sections of substrate 1, respectively, and are exemplary only. Such information is conventionally gathered when substrate 1 is in raw form and prior to any of the processing operations have been performed upon the substrate 1. A number of plots 11 may be taken at various locations and in various directions along the surface of substrate 1 to provide for the topographical mapping of the substrate.

[0021] FIG. 3 is a cross-sectional view of exemplary substrate 1. Substrate 1 may be any of various substrates such as an N- or P- type silicon substrate, a gallium arsenide substrate, a sapphire substrate or other substrates commonly used in the semiconductor manufacturing industry. Such substrates upon which semiconductor devices are to be formed, are also referred to as wafers in the semiconductor manufacturing industry. Substrate 1 includes substrate surface 3 upon which semiconductor devices are to be formed. Substrate surface 3 is uneven and includes raised sections 5 and depressed sections 7. As shown in FIG. 2, substrate 1 is generally round and may include a diameter 9 that may be 4, 6, 8, 10 or 12 inches or greater, in various exemplary embodiments.

[0022] FIG. 4 shows the structure shown in FIG. 3, after layer 13 has been formed over surface 3 of substrate 1. Layer 13 may consist of a single film or a plurality of films and one or more patterned layers may be included within layer 13. For example, layer 13 may represent an interlevel dielectric (ILD) that covers a patterned polysilicon or other film that forms interconnect leads. Layer 13 may also represent a film or plurality of films that have been polished using conventional methods. Such conventional polishing methods planarize structures locally but not necessarily globally over the surface of substrate 1. As such, upper surface 15 of layer 13 may generally include the same contours as original substrate surface 3 while local areas of upper surface 15 are substantially planarized.

[0023] FIG. 5 shows the structure in FIG. 4 after non-metallic layer 19 has been formed over upper surface 15. Non-metallic layer 19 is a non-reflective, light absorbing material and may be a dielectric layer such as an intermetal dielectric (IMD). Various suitable non-reflective materials may be used for non-metallic film 19 which includes top surface 21. Various suitable dielectric materials may be used in the exemplary embodiment in which non-metallic film 19 is an IMD. While various films such as non-metallic layer 19 may themselves include non-uniformities, such non-uniformities are typically within the range of hundreds or thousands of angstroms whereas the undulations in the substrate surface topography may be several microns. As such, the typical non-uniformities associated with non-metallic film 19 (or other formed films) will

generally be negligible when compared to differences in the substrate surface topography.

[0024] FIG. 6 shows the structure in FIG. 5 after a metal film 25 has been formed over non-metallic film 19. Metal film 25 may be copper or various other suitable
5 conductive materials. In an exemplary production embodiment, non-metallic film 19 may be an IMD and, on a local scale, metal film 25 may also extend within trenches, vias, or other openings formed within this IMD, but these are not shown as they are of negligible dimension, e.g. in the micron or even nanometer range, in comparison to substrate diameter 9 which is several inches. Metal films are reflective and therefore
10 the arrangement of metal film 25 formed over non-metallic film 19 may be alternatively considered a reflective film 25 formed over non-metallic film 19.

[0025] The substrate shown in FIG. 6 is then polished, for example, by using a conventional CMP (chemical mechanical polishing) operation. More particularly, surface 27 of metal film 25 is polished and locally planarized. In an exemplary
15 embodiment in which non-metallic film 19 is an intermetal dielectric, such a polishing operation may be used to remove metal film 25 from over top surface 21 of the intermetal dielectric while leaving metal within the aforementioned trenches, vias, and other openings formed in the intermetal dielectric to produce interconnect features.

[0026] FIG. 7 shows the substrate during an exemplary stage in the polishing
20 process. It can be seen that portions of metal film 25 have been removed in regions 33 in which top surface 21 of non-metallic film 19 is exposed. During the polishing operation, polished surface 31 is produced. Polished surface 31 also includes portions 35 in which metal film 25 still remains. It can be seen that metal remains in low topographical areas of substrate 1 (regions 7 in FIG. 3) and is first removed from
25 relatively high topographical areas of substrate 1 (regions 5 in FIG. 3). The polishing process may be continued until essentially all of metal film 25 that is above top surface 21 of non-metallic film 19, is removed.

[0027] The present invention provides for an optical profiling technique to be carried out during the polishing process. The optical profiling technique of the present
30 invention may be carried out at the instant of time illustrated in FIG. 7, for example. The

optical profiling technique of the present invention monitors polished surface 31 and distinguishes regions in which metal remains, from other regions in which the metal has been removed and the non-reflective non-metallic film exposed. Metallic (reflective) areas are thereby spatially distinguished from non-metallic (light absorbing) areas, thereby providing information on the topography of the raw substrate 1.

[0028] An optical beam is directed toward the substrate, more particularly, toward upper polished surface 31 and is used in detecting the presence or absence of metal film 25 which is reflective. An interferometer such as interferometer 51 may be used, but other arrangements for directing a light beam to polished surface 31 may be used in other exemplary embodiments. At location 33 where non-metallic film 19 is exposed and metal film 25 has been removed, beam 41 extends into non-reflective, non-metallic film 19 and provides refracted beam 43 that may be directed back to, and sensed by, interferometer 51. In areas such as region 35, in which metal remains, beam 45 is directed to surface 31 by an interferometer (not shown) which may be the same interferometer that produces beam 41. At polished surface 31, beam 45 is reflected to produce reflected beam 47 and a conventional interferometer does not detect a change in the optical signal. The interferometer distinguishes refracted beam 43, indicative of an exposed region of non-reflective, non-metallic material, from reflected beam 47, indicative of a metal region. Beams 41 and 43 are representative of optical beams directed to the substrate. In an exemplary embodiment, a number of beams may be directed toward multiple spatially separated locations over surface 31 and in another exemplary embodiment, a single beam may scan the surface. At a plurality of spatially separated locations along the substrate surface, the interferometer monitors the beam directed to the substrate surface and determines whether metal is still present or has been removed. Multiple scans along various directions may be made to provide a sample sufficient to map the entire substrate surface.

[0029] The optical profiling technique of the present invention may be repeated at various times during the polishing process, for example, before or after the exemplary instant of time illustrated in FIG. 7. The optical profiling technique of the present invention may be carried out periodically or substantially continuously throughout the

polishing operation, that is, a plurality of scans may be made at closely spaced time intervals during the polishing operation. When a plurality of such samplings are done over time and over the substrate surface, a two-dimensional scan of the substrate surface may be produced and displayed such as shown in FIGS. 1A and 1B.

5 Alternatively, a three dimensional topographical map of the substrate surface is achievable based on the locations and relative times in which top surface 21 of non-metallic film 19 is exposed. Regions where top surface 21 of non-metallic film 19 is first exposed, generally correspond to raised sections 5 such as shown in FIG. 3 and regions in which metal is last removed correspond to depressed section 7, such as
10 shown in FIG. 3.

[0030] In one exemplary embodiment, the interferometer may monitor the optical signals at scribe line locations along the substrate surface of a production wafer. Scribe lines 53 bound and separate semiconductor devices 55 on substrate 1, as shown in FIG. 8. In other exemplary embodiments, the interferometer may monitor the optical
15 signals every 5 or 10 mm, but other sampling schemes may be used in other exemplary embodiments.

[0031] Surface topography data of the raw substrate is thereby generated using the information obtained by scanning the substrate during the polishing process. Two or three dimensional wafer maps may be generated showing the spatial relationship of
20 the relative high and relative low areas of the raw substrate. In one exemplary embodiment, pass/fail criteria for acceptable surface topography variations may be inputted into and stored by the detecting/monitoring system or an electronic circuit associated with the detecting/monitoring system, and the surface topography data compared to the pass/fail criteria. In another exemplary embodiment, the raw substrate
25 topography profile may be compared to various other parameters and device characteristics which may vary across the surface of the substrate. From such a comparison, it may be determined that the undulations of the substrate surface correlate to the variations in the parameters and device characteristics. This detecting and monitoring may advantageously be carried out during the polishing process and as
30 such, in-line monitoring of the substrates is achieved. Alternatively, such comparative

data may direct one to other root causes of the various problems and anomalies. In response, various process controls and processing changes may be instituted to correct the cause of the problem or variation.

[0032] The present invention also provides an apparatus for carrying out the method described above. The apparatus may be used for in-line monitoring of substrates and is shown in FIG. 9. Apparatus 100 includes polishing means 106 such as a CMP apparatus and further includes a body 104 which may be a chuck, that receives substrate 102 to be polished. The apparatus also includes detecting means 114 that detect the presence or absence of a metal or reflective film, as opposed to a non-metallic or non-reflective film. As described above, detecting means 114 may be an optical device such as an interferometer and can read various locations across the substrate surface several times during the polishing operation. The apparatus further includes display means 110 such as a two-dimensional wafer profile such as shown in FIGS. 1A or 1B, or a three-dimensional wafer map such as shown in FIG. 2. Various other suitable display means known in the art may be used in other embodiments. The apparatus may include electronic circuitry 108 that may receive and store pass/fail criteria and automatically indicates whether the displayed substrate profile or map, satisfies the pass/fail criteria.

[0033] The preceding merely illustrates the principles of the invention. It will thus be appreciated that those skilled in the art will be able to devise various arrangements which, although not explicitly described or shown herein, embody the principles of the invention and are included within its spirit and scope. Furthermore, all examples and conditional language recited herein are principally intended expressly to be only for pedagogical purposes and to aid the reader in understanding the principles of the invention and the concepts contributed by the inventors to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions. Moreover, all statements herein reciting principles, aspects, and embodiments of the invention, as well as specific examples thereof, are intended to encompass both structural and functional equivalents thereof. Additionally, it is intended that such equivalents include both currently known equivalents and

equivalents developed in the future, i.e., any elements developed that perform the same function, regardless of structure.

[0034] This description of the exemplary embodiments is intended to be read in connection with the figures of the accompanying drawing, which are to be considered part of the entire written description. In the description, relative terms such as "lower," "upper," "horizontal," "vertical," "above," "below," "up," "down," "top" and "bottom" as well as derivatives thereof (e.g., "horizontally," "downwardly," "upwardly," etc.) should be construed to refer to the orientation as then described or as shown in the drawing under discussion. These relative terms are for convenience of description and do not require that the apparatus be constructed or operated in a particular orientation. Terms concerning attachments, coupling and the like, such as "connected" and "interconnected," refer to a relationship wherein structures are secured or attached to one another either directly or indirectly through intervening structures, as well as both movable or rigid attachments or relationships, unless expressly described otherwise.

[0035] Although the invention has been described in terms of exemplary embodiments, it is not limited thereto. Rather, the appended claims should be construed broadly, to include other variants and embodiments of the invention, which may be made by those skilled in the art without departing from the scope and range of equivalents of the invention.